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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/766,899	01/30/2004	Kenji Ichikawa	740165-371	5697

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NIXON PEABODY, LLP
401 9TH STREET, NW
SUITE 900
WASHINGTON, DC 20004-2128

EXAMINER	
CAO, PHAT X	
ART UNIT	**PAPER NUMBER**
2814	

DATE MAILED: 10/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/766,899	ICHIKAWA, KENJI	
	Examiner	Art Unit	
	Phat X. Cao	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) *6* is/are withdrawn from consideration.

5)☒ Claim(s) *5,7,8,10,12 and 14* is/are allowed.

6)☒ Claim(s) *1,2,4,9,11 and 13* is/are rejected.

7)☒ Claim(s) *3* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/30/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election with traverse of Group II (claims 1-5 and 9-14) in the reply filed on 7/25/05 is acknowledged. The traversal is on the ground(s) that "Applicant hereby elects the species of Group II ... with traverse". This is not found persuasive because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement.

The requirement is still deemed proper and is therefore made FINAL.

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1, 4 and 11 are rejected under 35 U.S.C. 102(b) as being anticipated by Huang et al (US. 6,157,065).

Regarding claim 1, Huang (Fig. 2) discloses a semiconductor device comprising: a first MOS transistor group including a first gate electrode 29 (left gate electrode 29) and a first impurity diffused layer 26; a second MOS transistor group including a second gate electrode 29 (right gate electrode 29), which is arranged in parallel with the first

gate electrode 29 (left gate electrode 29), and a second impurity diffused layer 26; input ground signal wiring Vss, to which an input signal is applied, disposed between the first MOS transistor group and the second MOS transistor group 29; and a conducting portion (corresponding to the horizontal portion of wiring 28) extending on the first and second impurity diffused layers 26 for electrically connecting the first and the second gate electrodes 29 to the input signal wiring Vss.

Regarding claim 4, Huang (Fig. 2) further discloses an interlayer insulating layer (not labeled) disposed between the conducting portion (horizontal portion of 28) and the input signal wiring Vss, the interlayer insulating layer being provided with a contact 28 (vertical portion of 28) for electrically connecting the conducting portion to the input signal wiring Vss.

Regarding claim 11, Huang (Fig. 2) further discloses that the conducting portion (horizontal portion of 28 in Fig. 2 or horizontal portion 414 in Fig. 4C) is a silicide layer (column 3, lines 27-33).

5. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Rhee (US. 6,365,941).

Rhee (Fig. 5) discloses a semiconductor device comprising: a first MOS transistor group including a first gate electrode 15 (left gate electrode 15) and a first impurity diffused layer 21a; a second MOS transistor group including a second gate electrode 15 (right gate electrode 15), which is arranged in parallel with the first gate electrode 15, and a second impurity diffused layer 21a; input signal wiring 29p (corresponding to the vertical portion of 29p formed within the insulating layer 28), to

which an input signal is applied (column 8, lines 65-67), disposed between the first MOS transistor group and the second MOS transistor group 15; and a conducting portion 29p (corresponding to the horizontal portion of 29p formed on the insulating layer surface 28) extending on the first and the second impurity diffused layers 21a for electrically connecting the first and the second gate electrodes 15 to the input signal wiring 29p (vertical portion 29p).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 2 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rhee (US. 6,365,941) in view of Applicant's admitted prior art.

As discussed above, Rhee (Fig. 5) discloses an integrated circuit device including a first transistor used in an output circuit and a second transistor used in an internal circuit for receiving the signal from a signal pad and transmitting the electrical signal to the internal circuit (column 8, lines 65-67), the first transistor comprises: a semiconductor device comprising: a first MOS transistor group including a first gate electrode 15 (left gate electrode 15) and a first impurity diffused layer 21a; a second MOS transistor group including a second gate electrode 15 (right gate electrode 15), which is arranged in parallel with the first gate electrode 15, and a second impurity diffused layer 21a; input signal wiring 29p (corresponding to the vertical portion of 29p

formed within the insulating layer 28), to which an input signal is applied (column 8, lines 65-67), disposed between the first MOS transistor group and the second MOS transistor group 15; and a conducting portion 29p (corresponding to the horizontal portion of 29p formed on the insulating layer surface 28) extending on the first and the second impurity diffused layers 21a for electrically connecting the first and the second gate electrodes 15 to the input signal wiring 29p (vertical portion 29p).

Rhee does not disclose that the second transistor comprises a salicide MOS transistor.

However, Applicant's admitted prior art (Fig. 7B) teaches the convention salicide MOS transistors having the silicide source/drain regions 170/171/172 spaced apart by a predetermined distance from the gate electrodes. Accordingly, it would have been obvious to form the second MOS transistor as a salicide MOS transistor because such forming a structure of salicide MOS transistor is well known in the art for providing the MOS transistor having low resistance (see Applicant's specification, page 6, third paragraph).

8. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Rhee (US. 6,365,941) in view of Tago et al (US. 2005/0179057).

Rhee (Fig. 5) further discloses that the gate electrodes 15 comprise polysilicon (column 13, lines 55-58).

Rhee does not disclose that the wiring conducting portion 29p (horizontal portion) comprises polysilicon.

However, Tago teaches the forming of a wiring conducting portion made of polysilicon or aluminum for connecting the gates to each other (par. [0083]). Accordingly, it would have been obvious to form the wiring conducting portion 29p of Rhee with either metal or polysilicon because they are both well known materials having conductivity characteristics, as taught by Tago (par. [0083]).

Allowable Subject Matter

9. Claim 3 is objected to as being dependent upon a rejected base claim; but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The prior art of record fails to disclose that the conducting portion is formed in the same layer as the first and the second gate electrodes and extends from the first gate electrode to the second gate electrode.

10. Claims 5, 10, 12 and 14 are allowed.

The prior art of record fails to disclose all the limitations recited in the base claims, including the combination of a semiconductor device structure comprising: first and second MOS transistor groups; and a contact formed in the interlayer insulating layer for electrically connecting the input signal wiring to the conducting portion , the contact is formed outside of an active region including the gate electrodes and the impurity diffused layers.

11. Non-elected claims 7-8 are also allowed because they are generic to allowable independent claim 5.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phat X. Cao whose telephone number is 571-272-1703. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PC
September 30, 2005

PHAT X. CAO
PRIMARY EXAMINER